UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,366	01/14/2004	Hiroaki Nakano	TAI 146	2358

23995 7590 08/16/2005

RABIN & Berdo, PC
1101 14TH STREET, NW
SUITE 500
WASHINGTON, DC 20005

EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding..

Office Action Summary	Application No.	Applicant(s)
	10/756,366	NAKANO, HIROAKI
	Examiner	Art Unit
	Ori Nadav	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/05/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-8 and 16-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of a surface including regions, wherein the regions (i.e. the surface) including a semiconductor chip region on the surface (i.e. on the regions), as recited in claims 1 and 6, are unclear as to whether the semiconductor chip region is included in the regions (i.e. in the surface) or the semiconductor chip region is located on the regions (i.e. on the surface).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 6, 9, 12-13 and 15-18, as best understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Baba (6,046,077).

Baba teaches in figure 5 and related text a circuit board for mounting a semiconductor chip, the circuit board including

an insulating substrate 4 having a surface, the surface including mutually non-overlapping regions, the regions including

a semiconductor chip region 1 on the surface of the insulating substrate for mounting the semiconductor chip, and

at least one wiring region 12 on the surface of the insulating substrate in which wirings electrically connectable to the semiconductor chip are formed, and

at least one reinforcement layer region 6 on the surface of the insulating substrate in which reinforcement layers for maintaining the strength of the circuit board for mounting the semiconductor chip are formed; and

a protective film 3 that covers the wirings.

Regarding claims 2-3 and 12-13, Baba teaches a semiconductor chip that covers part of the wiring region, wherein the reinforcement layers comprise copper wirings (column 1, lines 38-39).

Regarding claim 9, Baba teaches in figure 5 and related text a circuit board for mounting a semiconductor chip, the circuit board comprising:

an insulating substrate, the insulating substrate having a top surface and a bottom surface, with the top surface including mutually separated first, second and third regions on the insulating substrate;

wirings provided in the second region on the top surface of the insulating substrate, with the semiconductor chip being electrically connected to the wirings;

reinforcement layers provided only in the third region on the top surface of the insulating substrate, with the reinforcement layers maintaining the strength of the circuit board for mounting a semiconductor chip;

a protective film formed on the insulating substrate so as to cover the wirings and the reinforcement layers; and

the semiconductor chip mounted on the protective film above the first region on the top surface of the insulating substrate,

wherein the third region encloses the first region and the second region (see figure 4A).

Regarding claims 15-18, Baba teaches in figure 5 and related text solder balls 8 that are disposed on the bottom surface of the insulating substrate and electrically connected to the wirings, wherein the wiring region is disposed in a vicinity of the semiconductor chip region and the reinforcement layer region is disposed in vicinity of the wiring region, wherein the wiring region (the region that includes wirings 15 and located between the semiconductor chip region and the reinforcement layer region) is disposed between the semiconductor chip region and the reinforcement layer region, and wherein the reinforcement layer region encloses the wiring region and the semiconductor chip region.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baba in view of Lin et al. (6,534,852).

Baba teaches substantially the entire claimed structure, as applied to claim 1 above, except a protective film being planarized.

Lin et al. teach in figure 5 a protective film being planarized. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to planarize the protective film of Baba's device in order to reduce warpage and defect generation.

Claims 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baba in view of Norville (6,534,852).

Baba teaches substantially the entire claimed structure, as applied to claims 1 and 6 above, except a protective film being planarized by cutting and polishing.

Norville teaches in figure 5 a protective film being planarized by cutting and polishing (column 4, lines 34-38). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to planarize the protective film of Baba's device by cutting and polishing, in order to reduce warpage and defect generation.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baba in view of Applicant Admitted Prior Art (AAPA).

Baba teaches substantially the entire claimed structure, as applied to claim 9 above, except a protective film is a solder resist.

AAPA teaches a protective film is a solder resist (page 2, lines 3-4 and 20-23). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a protective film of a solder resist in Baba's device in order to obtain a protective mask for efficient packaging.

Claims 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baba in view of Niwa (6,259,154).

Baba teaches substantially the entire claimed structure, as applied to claims 1 and 9 above, except reinforcement layers comprise insulating materials, and wherein the semiconductor chip region does not overlap the wiring region.

Niwa teaches in figure 2 reinforcement layers comprise insulating materials, and in figure 6 the semiconductor chip region does not overlap the wiring region. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use reinforcement layers comprise insulating materials, and wherein the semiconductor chip region does not overlap the wiring region, in Baba's device in order

to reduce the weight of the package and in order to simplify the processing steps of making the device.

Response to Arguments

Applicant's arguments with respect to claims 1-19 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
8/15/05

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800